

**PATENT**  
**72370/10175**

What is claimed is:

1. A method of protecting Flash memory against alterations, comprising providing different degrees of protection including persistently locking a sector for preventing modification of the sector, and  
5 dynamically locking a sector which prevents modification of the sector without first resetting a protection bit.
2. A method of Claim 1, wherein persistently locking a sector, includes assigning a persistent protection bit (PPB) in non-volatile memory.
3. A method of Claim 1, wherein dynamically locking a sector, includes assigning a  
10 dynamic protection bit (DPB) in a volatile memory. This volatile memory may take the form of flip-flops.
4. A method of Claim 3, wherein the DPBs are individually modifiable through a write command.
5. A method of Claim 3, wherein after a power-up or a hardware reset all DPBs are  
15 either set or reset, depending on the desired default state.
6. A method of Claim 2, further comprising a further level of protection applying to the persistent locking of the sectors, by making use of a PPB lock bit in volatile memory, which, when set, prevents the states of the PPBs being changed.
7. A method of Claim 1, further comprising holding a write protect pin low to  
20 prevent certain sectors being changed.
8. A method of Claim 7, further comprising maintaining boot code in said certain sectors.
9. A method of Claim 6, further comprising including a password mode requiring that a password be entered in order to clear the PPB lock bit.
- 25 10. A method of Claim 9, wherein the password is a fixed password.
11. A method of Claim 9, wherein the password is variable and is produced by a dynamic password algorithm.
12. A method of Claim 9, wherein when password mode is selected, the PPB lock bit is in a set state when the device is first powered on or comes out of a reset cycle.
- 30 13. A method of Claim 10, wherein the password is stored in a one time programmable region of the Flash memory.

14. A method of Claim 9, wherein a password mode locking bit is assigned which permanently sets the Flash memory in password mode.

15. A method of Claim 9, wherein a non-password mode locking bit is assigned which, once set, permanently prevents entering the password mode.

5 16. A method of Claim 9, wherein a time delay is introduced between each attempt to clear the PPB lock bit.

17. A method of Claim 9, wherein only a limited number of successive attempts at clearing the PPB lock bit are permitted.

10 18. A method of Claim 9, wherein a new power cycle is required between attempts to clear the PPB lock bit.

19. A method of Claim 9, wherein the password is related to an electronic serial number (ESN) of the Flash memory.

15 20. A Flash memory having multiple degrees of protection, comprising  
a non-volatile storage area defining at least one Persistent Protection Bit (PPB)  
which has to be cleared in order to change the contents of the memory, and  
a volatile storage area defining at least one Dynamic Protection Bit (DPB), which  
has to be cleared in order to change the contents of the memory.

21. A method of Claim 20, wherein the volatile storage area further defines at least one PPB lock bit which, when set prevents the at least one PPB from being cleared.

20 22. A method of Claim 21, wherein each DPB and each PPB lock bit can be cleared only by means of a power-up or hardware reset.

23. A method of Claim 21, wherein there is one PPB and one DPB per sector of the Flash memory, and a single global PPB lock bit for all sectors.

25 24. A Flash memory includes a password or password generating code in the non-volatile storage area in an area that is read and write protected.

25. A method of Claim 24, wherein the password in the non-volatile storage area or generated by the code defines a password that has to be entered to clear the PPB lock bit.

26. A method of Claim 25, wherein the Flash memory includes at least one mode selection bit for selecting password mode or non-password mode.

**PATENT**  
**72370/10175**

27. A method of Claim 26, wherein the at least one mode selection bit is located in a one time programmable portion of the memory to permanently lock the memory into one or the other mode.

28. A method of Claim 20, wherein further including a write protect pin to prevent  
5 programming or erasing of part of the Flash memory.